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09/510,375	02/22/2000	Brett L. Williams	303.164US3	3060

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EXAMINER	
KIM, HONG CHONG	

ART UNIT	PAPER NUMBER
2186	28

DATE MAILED: 05/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/510,375	WILLIAMS, BRETT L.	
	Examiner	Art Unit	
	Hong C Kim	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *26-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Detailed Action

1. Claims 26-52 are presented for examination. This office action is in response to the amendment filed on 3/3/04.

Claim Objections

2. Claims 50-52 are objected to because of the following informalities: As to claim 50, it is unclear dependency of this claim, since claim 1 does not exist. Appropriate correction is required.

Claim Rejections - 35 USC § 102/103

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 26, 29, 32, 35-39, 40 and 50-52 are rejected under 35 U.S.C. 102(e) as being anticipated by Langendorf et al. (Langendorf) US Patent No. 6,505,282 or, in the

alternative, under 35 U.S.C. 103(a) Langendorf et al. (Langendorf) US Patent No. 6,505,282 in view of Margulis et al. (Margulis) U.S. Patent No. 5,392,239.

As to claims 26, 29, 32 and, 35-39, Langendorf discloses the invention as claimed. Langendorf discloses a system (Fig. 1) comprises a bus (Fig. 1 Ref. 101), a memory (Fig. 2 Ref. 103), coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of burst EDO (Fig. 4 and col. 6 lines 34-39, burst read reads on this limitation) and fast page mode (abstract and Figs. 2, 3, 4 and 5), the memory having a first set and second set of access signal timing requirements (Figs. 3, 4 and 5), a memory controller (col. 3 lines 60-63) capable of providing the first set access control signal timing requirement and the second set access control signal timing requirement (Fig. 2) and a processor (Fig. 2 Ref. 102) responsive to at least information from the memory program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device (Fig. 5).

Even if the system does not include a burst mode operation. It was well known in the memory art to include the burst mode operation in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every CAS cycle.

Margulis discloses the bust mode operation (Fig. 5 and Fig. 6, and col. 3 lines 58+) for the purpose of providing a new internal column address every CAS cycle after an initial column address (Fig. 5 and Fig. 6 Refs. 172-174) thereby increasing the throughput .

One of ordinary skill in the memory art familiar with Langendorf, and looking at Margulis would have recognized that the memory access performance of Langendorf would have been enhanced by including a burst mode in the memory because it would provide a new internal column address every CAS cycle thereby increasing the memory throughput or speed. The ability to provide a new internal column address every cycle after an initial column address would have a highly desirable feature in the memory environment of Langendorf because one of the objectives of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a burst mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the memory selectively operable in a burst mode of Margulis in the invention of Langendorf because it would increase memory performance of Langendorf by providing a new internal column address every CAS cycle thereby increasing the memory throughput or speed in Langendorf.

As to claim 36, Langendorf or Langendorf and Margulis disclose(s) the invention as claimed above. Langendorf further discloses the memory type of the second bank is interchangeable (abstract and col. 3 lines 30-33).

As to claims 50, 51 and 52, Langendorf or Langendorf and Margulis disclose(s) the invention as claimed above. Margulis further discloses toggling a CAS and internal counter (col. 3 lines 58+).

4. Alternatively, Claims 26, 29, 32, 35-39, and 40 are rejected under 35 U.S.C. 102(a) as being anticipated by Intel Electronic News, (EN) December 5, 1994 in view of 82430FX PCIset DATASHEET 82437FX System CONTROLLER (TSC) AND 82438FX DATA PATH UNIT (TDP), Intel Corp., pp 1-67, 11/96 (INTEL) or, in the alternative, under 35 U.S.C. 103(a) Intel Electronic News, (EN) December 5, 1994 in view of 82430FX PCIset DATASHEET 82437FX System CONTROLLER (TSC) AND 82438FX DATA PATH UNIT (TDP), Intel Corp., pp 1-67, 11/96 (INTEL) further in view of Margulis et al. (Margulis) U.S. Patent No. 5,392,239.

As to claims 26, 29, 32 and, 35-39, *EN* discloses the invention as claimed. *EN* discloses Triton PCI Chip set. It is inherent that a computer system comprising a processor, a bus, a memory system including the first and second memory devices are page mode memory and the Burst EDO memory (Page 1 and page 45 table 11) respectively, a memory controller capable of providing the first set access control signal timing requirement and the second set access control signal timing requirement. These inherent features are disclosed by Intel (Fig. 1 and pp 1, 24, 31, and 41-45).

See MPEP 2124 and 2131.01 for multiple reference 35 U.S.C. 102 rejections.

Even if the system does not include a burst mode operation. It was well known in the memory art to include the burst mode operation in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every CAS cycle.

Margulis discloses the bust mode operation (Fig. 5 and Fig. 6, and col. 3 lines 58+) for the purpose of providing a new internal column address every CAS cycle (Fig. 5 and Fig. 6 Refs. 172-174) after an initial column address thereby increasing the throughput.

One of ordinary skill in the memory art familiar with EN and Intel, and looking at Margulis would have recognized that the memory access performance of EN and Intel would have been enhanced by including a burst mode in the memory because it would provide a new internal column address every CAS cycle thereby increasing the memory throughput or speed. The ability to provide a new internal column address every cycle after an initial column address would have a highly desirable feature in the memory environment of EN and Intel because one of the objectives of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a burst mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the memory selectively operable in a burst mode of Margulis in the invention of EN and Intel because it would increase memory performance of EN and Intel by providing a new internal column address every CAS cycle thereby increasing the memory throughput or speed in EN and Intel.

Claim Rejections - 35 USC ' 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 27-28, 30-31, 33, 34, and 41-52 are rejected under 35 U.S.C. 103(a) as being anticipated by Langendorf et al. (Langendorf) US Patent No. 6,505,282 or, in the alternative, under 35 U.S.C. 103(a) Langendorf et al. (Langendorf) US Patent No. 6,505,282 in view of Margulis et al. (Margulis) U.S. Patent No. 5,392,239 and further in view of Suzuki et al. (Suzuki) US Patent No. 5,787,308.

As to claims 27-28, 30-31, 33, 34, and 41-49, Langendorf or Langendorf and Margulis disclose the invention substantially as claimed in the above claim. Langendorf further discloses during the initialization a signal to cause the processor to detect the memory device mode and to program the memory controller (col. 5 lines 20+). Although Langendorf or Langendorf and Margulis discloses that configuration information is loaded into each of the registers during the initialization of the computer system and any subsequent addition of a DRAM device to the computer system after initialization (col. 5 lines 25-30) and during a normal system boot operation of computer system 100, the system BIOS (not shown) configures boot registers to configure the

various memory banks in the system. The system BIOS then presents this information to the configuration registers 300 to be stored so that the memory controller knows the contents of each bank of memory in the system (i.e., whether a bank contains EDO or standard DRAM) (col. 5 line 45-52), however, Langendorf or Langendorf and Margulis does not specifically discloses a power supply and a power up detection circuit coupled to the processor and to the power supply.

Suzuki disclose a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to start initialization (col. 7 lines 48+) for the purpose of determining a computer configuration thereby guaranteeing reliable operation of the system. Also it would have been readily appreciated by one of ordinary skill in the art that a system includes a power supply to provide a power to the system.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the power supply and a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller of Suzuki into the invention of Langendorf or Langendorf and Margulis for the advantages stated above.

As to claims 50, 51 and 52, Margulis further discloses toggling a CAS and internal counter (col. 3 lines 58+).

6. Alternatively, Claims 27-28, 30-31, 33, 34, and 41-52 are rejected under 35 U.S.C. 103(a) as being anticipated by Intel Electronic News, (EN) December 5, 1994 in view of 82430FX PCIset DATASHEET 82437FX System CONTROLLER (TSC) AND 82438FX DATA PATH UNIT (TDP), Intel Corp., pp 1-67, 11/96 (INTEL) or, in the alternative, under 35 U.S.C. 103(a) Intel Electronic News, (EN) December 5, 1994 in view of 82430FX PCIset DATASHEET 82437FX System CONTROLLER (TSC) AND 82438FX DATA PATH UNIT (TDP), Intel Corp., pp 1-67, 11/96 (INTEL) further in view of Margulis et al. (Margulis) U.S. Patent No. 5,392,239 and further in view of Suzuki et al. (Suzuki) US Patent No. 5,787,308.

As to claims 27-28, 30-31, 33, 34, and 41-49, *EN and Intel* disclose the invention substantially as claimed in the above claim. Although Intel discloses that DRAM types are determined by BIOS (which implies that DRAM types are determined during an initialization (i.e. a power up) sequence and system includes a power up detection circuit to start a BIOS sequence), however, neither En nor Intel specifically discloses a power supply; and a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller; wherein the processor is responsive to at least information from the memory to program the memory controller to provide the first set of access control signals to the memory at a first time and the second set of access control signals to the memory at a second time.

Suzuki disclose a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller (col. 7 lines 48+) for the purpose of determining a computer configuration thereby guaranteeing reliable operation of the system. Also it would have been readily appreciated by one of ordinary skill in the art that a system includes a power supply to provide a power to the system.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the power supply and a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller of Suzuki into the combined invention of EN and Intel for the advantages stated above.

As to claims 50, 51 and 52, Margulis further discloses toggling a CAS and internal counter (col. 3 lines 58+).

7. Claims 26, 29, 32, 35-39, and 50-52 are rejected under 35 U.S.C. 103(a) as being anticipated by Farrer et al. (Farrer) US Patent No. 5,307,320 in view of Micron, "Reduce DRAM cycle times with extended data-out", Micron technical Note pp 5-33 thru 5-40, 4/94 and further in view of Margulis et al. (Margulis) U.S. Patent No. 5,392,239.

As to claims 26, 29, 32, and 35-39, *Farrer* discloses a system, comprising:

a bus (Fig. 1 Ref. 105) for transferring information;

a memory (Fig. 1 Ref. 103), coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of a first mode (Fig. 3 Ref. 301) and a second mode (Fig. 3 Ref. 302), the memory having a first set of access control signal timing requirements for the first mode and a second set of access control signal timing requirements for the second mode;

a programmable memory controller (col. 5 lines 16 and 54-66), coupled to the bus and to the memory, capable of providing the first set of access control signal timing requirements and the second set of access control signal timing requirements to the memory; and

a processor (Fig. 1 Ref. 101), coupled to the bus and the memory controller, responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device.

However Farrer does not specifically disclose a memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of extended data out mode and fast page mode, the memory having a first set of access control signal timing requirements for the extended data out mode and a second set of access control signal timing requirements for the fast page mode. Micron discloses a memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of extended data out

mode and fast page mode, the memory having a first set of access control signal timing requirements for the extended data out mode and a second set of access control signal timing requirements for the fast page mode (page 5-33 bottom of right column and page 5-39 bottom of right column) thereby the user may base the design of the computer system on the type of memory that offers the target price/performance ration of the system. *Micron* further discloses that the memory device is interchangeable (page 5-33 bottom of right column and page 5-39 bottom of right column).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of extended data out mode and fast page mode, the memory having a first set of access control signal timing requirements for the extended data out mode and a second set of access control signal timing requirements for the fast page mode of Micron in the invention of Farrer for the advantages stated above.

Furthermore neither Farrer nor Micron discloses a burst mode. However it is well known in the memory art a memory can be operate in a burst mode. For example Margulis discloses burst mode of operation (Figs. 5 and 6) in order to increase access time.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use burst access memory of Margulis in the combined invention of Farrer and Margulis for the purpose of increasing access time thereby increasing overall system performance.

As to claims 50, 51 and 52, Margulis further discloses toggling a CAS and internal counter (col. 3 lines 58+).

8. Claims 27-28, 30-31, 33, 34 and 41-49 are rejected under 35 U.S.C. 103(a) as being anticipated by Farrer et al. (Farrer) US Patent No. 5,307,320 Micron Reduce DRAM cycle times with extended data-out, Micron technical Note pp 5-33 thru 5-40, 4/94 and Margulis et al. (Margulis) U.S. Patent No. 5,392,239 and further in view of Suzuki et al. (Suzuki) US Patent No. 5,787,308.

As to claims 27-28, 30-31, 33, 34, and 41-49, *Farrer, Micron, and Margulis* disclose the invention substantially as claimed in the above claim. However, neither Farrer, Micron, nor Margulis specifically discloses a power supply; and a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to á signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller; wherein the processor is responsive to at least information from the memory to program the memory controller to provide the first set of access control signals to the memory at a first time and the second set of access control signals to the memory at a second time.

Suzuki disclose a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller (col. 7 lines 48+) for the purpose of determining a computer

configuration thereby guaranteeing reliable operation of the system. Also it would have been readily appreciated by one of ordinary skill in the art that a system includes a power supply to provide a power to the system.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the power supply and a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller of Suzuki into the combined invention of Farrer, Micron, and Margulis for the advantages stated above.

Response to Amendment

9. Applicant's arguments filed on 3/3/04 have been fully considered but they are not persuasive.

Applicant's remarks on pages 13-20, the references not showing a burst extended data out mode is not considered persuasive.

Langendorf discloses a burst EDO mode (Fig. 4 and col. 6 lines 34-39, burst read reads on this limitation).

Margulis also discloses the bust mode operation (Fig. 5 and Fig. 6, and col. 3 lines 58+)

Intel also discloses a burst EDO mode (Page 1 and page 45 Table 11).

Also in response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by

combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, even though applicant's modification results in great improvement and utility over the prior art, it may still not be patentable if the modification was within the capabilities of one skilled in the art. In re Sola, 22 C.C.P.A. (Patents) 1313, 77 F.2d 627, 25 USPQ 433 ; In re Normann et al., 32 C.C.P.A. (Patents) 1248, 150 F.2d 708, 66 USPQ 308 ; In re Irmscher, 32 C.C.P.A. (Patents) 1259, 150 F.2d 705, 66 USPQ 314.

Those skilled in memory art must be presumed to know something about memory mode apart from what references disclose; it is immaterial that reference does not disclose specific function set forth in applicant's specification, since this is merely a different variation which would be obvious to one skilled in the art in a use which one skilled in the art, following teachings of prior art, might make of it. In re JACOBY, 135 USPQ 317 (CCPA 1962).

Therefore, the rejections are proper.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

2. a shortened statutory period for response to this action is set to expire 3

(three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

3. Applicants are requested to number each line of each claim starting with line number one to provide easier communication in the future.

4. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

5. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

6. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to TC-2100: 703-872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong C Kim whose telephone number is 703-305-3835. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HK
Primary Patent Examiner
May 16, 2004